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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,111	06/26/2003	James Michael Devine	7650-0018	9252
51094	7590	11/18/2005	EXAMINER	
MCCORMICK, PAULDING & HUBER LLP 185 ASYLUM STREET CITY PLACE II HARTFORD, CT 06103			TON, MY TRANG	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

In response to Applicant's arguments, the rejection made in the last Office action on the Tsukahara reference (U.S Patent No. 5,592,108) and Turner (U. S Patent No. 6,118,302) is withdrawn.

In view of newly discovered prior art, new ground of rejection are now set forth. Any inconvenience caused by the delay in citing this new prior art is regretted. In view of the above noted new grounds of rejection not necessitated by Applicants Amendments, this action is non-final.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Pryor (U.S Patent No. 4,408,245).

Pryor discloses in Fig. 1 a protection and anti-floating network for insulated gate field effect circuitry including:

an active pull-up device (P12);

a level shift circuit (N12) coupled to the active pull-up device (P12) wherein the active pull-up device (P12) is coupled to a one-wire bus (wire connected to P12, N12)

Art Unit: 2816

and the level shift circuit (N12) is also coupled to circuit ground (Ground) as recited in claim 1.

Regarding claim 2, one connection point of the level shift circuit (N12) is coupled to a reference connection point (point connected between P12, N12) of the active pull-up device (P12) and another connection point of the level shift circuit (N12) is connected to circuit ground (Ground).

The active pull up device (P12) has a voltage sense switch (P12) that is coupled to the level shift circuit (N12) as recite in claim 3.

Regarding claim 4: the level shift circuit (N12) is a diode with its cathode connected to circuit ground and its anode connected to a reference connection point of the active pull-up device (N12 forms diode-connected configuration as recited in claim 4).

Regarding claim 5: elements ND2, ND3 read on at least one I-button device.

Regarding claim 6: elements P11, N11 read on a transceiver having a processor.

Claims 7-13 are similarly rejected as claims 1-6: a level shift (N12) and an active pull-up device (P12).

Claims 1-13 are also rejected under 35 U.S.C. 102(b) as being anticipated by Chung et al (U. S Patent No. 6,535,026).

Chung disclose in Fig. 3b a sense amplifier circuit including:

an active pull-up device (96);

a level shift circuit (102) coupled to the active pull-up device (96) wherein the active pull-up device (96) is coupled to a one-wire bus (wire connected to SA, VZ) and

Art Unit: 2816

the level shift circuit (102) is also coupled to circuit ground (Ground) as recited in claim 1.

Regarding claim 2, one connection point of the level shift circuit (102) is coupled to a reference connection point (node connected to 100) of the active pull-up device (96) and another connection point of the level shift circuit (102) is connected to circuit ground (Ground).

The active pull up device (96) has a voltage sense switch (96) that is coupled to the level shift circuit (102) as recite in claim 3.

Regarding claim 4: the level shift circuit is a diode with its cathode connected to circuit ground and its anode connected to a reference connection point of the active pull up device (102 forms a diode connected configuration as recited in claim 4).

Regarding claim 5: elements 116 & transistors connected to DE2 & 116 read on the limitation "at least one I-button device".

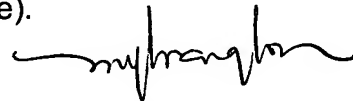
Regarding claim 6: transistors connected to DE1, DE1B and inverters connected to DE1B, DE1 inherently read on a transceiver having a processor.

Claims 7-13 are similarly rejected as claims 1-6.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
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Art Unit 2816

November 16, 2005